AN6912, AN6912S

Quadruple Comparators

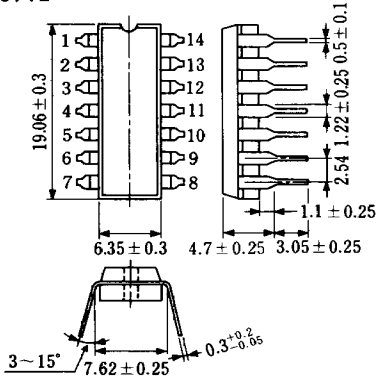
■ Outline

The AN6912 and the AN6912S are quadruple (voltage) comparators with wide range of operating supply voltages.

■ Features

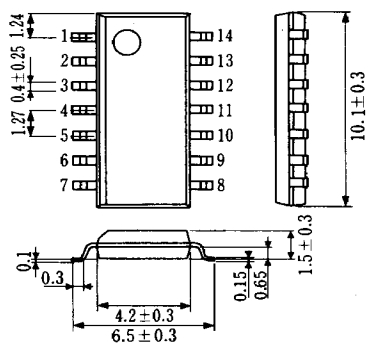
- Wide range of supply voltage
  Single supply : 2～36V
  Dual supply : ±1～±18V
- Low circuit current : 0.8mA typ.
- Wide range of common-mode input voltage
  0V～V_{CC}－1.5V (single supply)
- Open collector output

AN6912 Unit : mm



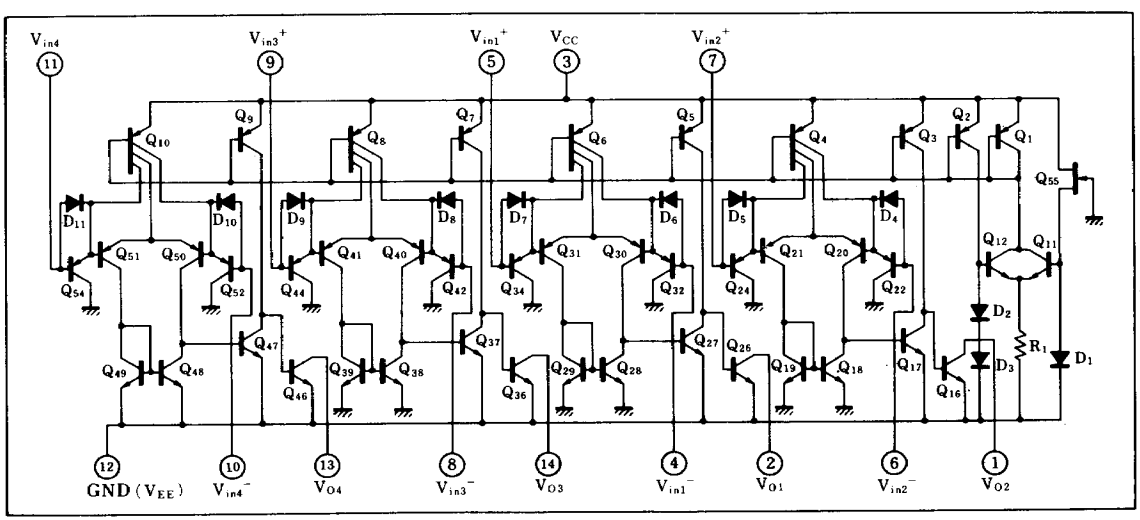
14-Lead DIL Plastic Package

AN6912S Unit : mm



14-Lead PANAFLAT Package(SO-14D)

■ Schematic Diagram



Panasonic

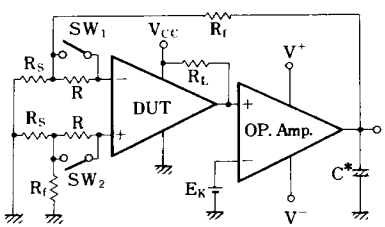
■ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Rating	Unit
Voltage	Supply Voltage	V_{CC}	36	V
	Common-Mode Input Voltage	V_{ICM}	−0.3～+36	V
	Differential Input Voltage	V_{ID}	36	V
Power Dissipation	AN6912	P_D	570	mW
	AN6912S		380	
Operating Ambient Temperature		T_{opr}	−20～+75	℃
Storage Temperature	AN6912	T_{stg}	−55～+150	℃
	AN6912S		−55～+125	

■ Electrical Characteristics (V_{CC}=5V, Ta=25±2℃)

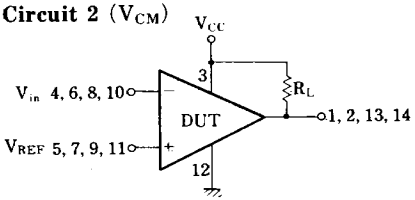
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	$V_{I(offset)}$	1			2	5	mV
Input Offset Current	I_{IO}	1				50	nA
Input Bias Current	I_{Bias}	1				250	nA
Voltage Gain	G_V	1	R_L=15kΩ		200		V/mV
Common-Mode Input Voltage Range	V_{CM}	2		0		V_{cc}−1.5	V
Supply Current	I_{CC}	3	R_L=∞		0.8	2	mA
Response Time	t_r	4	R_L=5.1kΩ, V_{RL}=5V		1.3		μs
Output Sink Current	I_{SINK}	5	R_{REF}=0V, V_I=1V, V_O≦1.5V	6			mA
Low-Level Output Voltage	V_{OL}	6	V_{REF}=0V, V_I=1V, $I_{(SINK)}$=3mA		0.2	0.4	V
Output Terminal Leakage Current	$I_{O(Leak)}$	7	V_I=0V, V_{REF}=1V, V_O=5V		0.1		nA

Test Circuit 1 ($V_{I(offset)}$, I_{IO}, I_{Bias}, G_V)

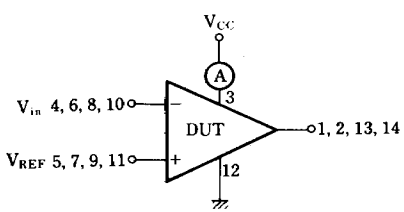


*Capacitors for the prevention of oscillation and bipolar should be used (NP).

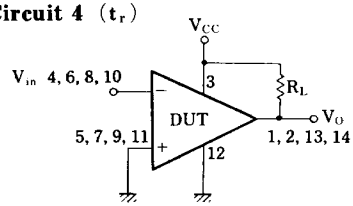
Test Circuit 2 (V_{CM})

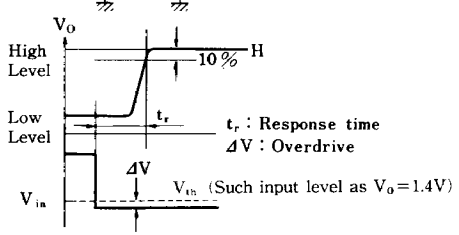


Test Circuit 3 (I_{CC})

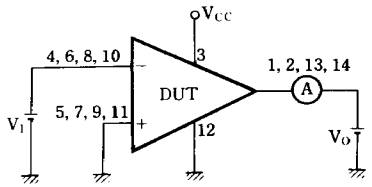


Test Circuit 4 (t_r)

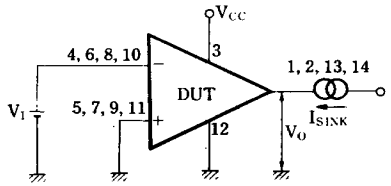




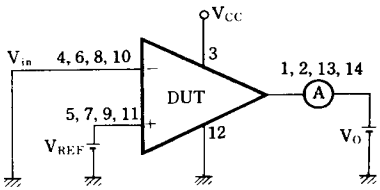
Test Circuit 5 (I_{SINK})



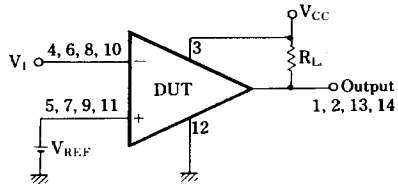
Test Circuit 6 (V_{OL})



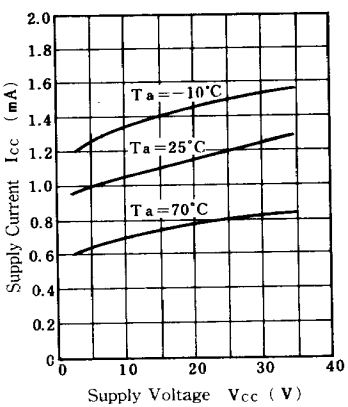
Test Circuit 7 ($I_{O(Leak)}$)



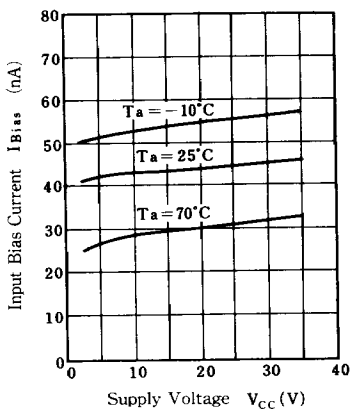
■ Application Circuit



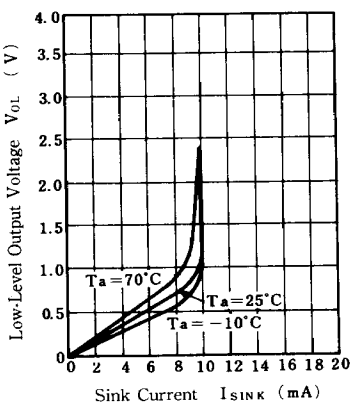
$I_{CC} - V_{CC}$



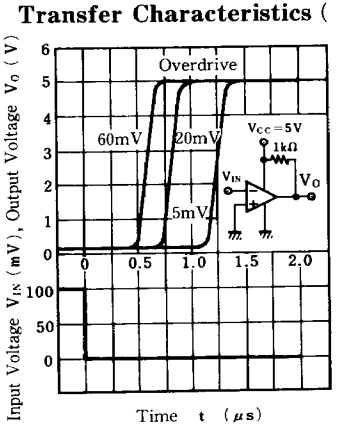
$I_{Bias} - V_{CC}$



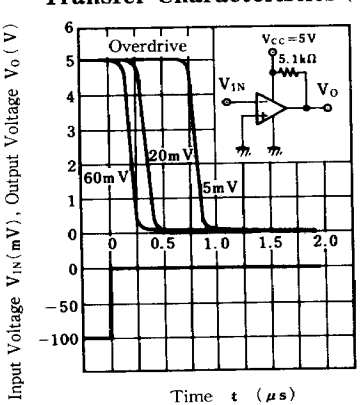
$V_{OL} - I_{SINK}$



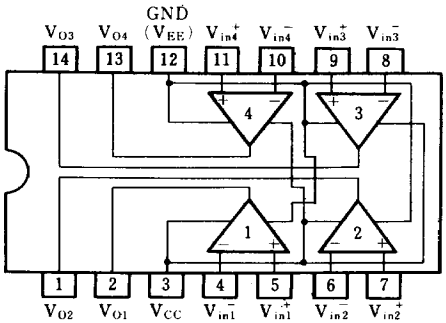
Transfer Characteristics (1)



Transfer Characteristics (2)



■ Block Diagram



■ Pin

Pin No.	Pin Name
1	Ch. 2 Output
2	Ch. 1 Output
3	V_{CC}
4	Ch. 1 Inverting Input
5	Ch. 1 Non Inverting Input
6	Ch. 2 Inverting Input
7	Ch. 2 Non Inverting Input
8	Ch. 3 Inverting Input
9	Ch. 3 Non Inverting Input
10	Ch. 4 Inverting Input
11	Ch. 4 Non Inverting Input
12	GND(V_{EE})
13	Ch. 4 Output
14	Ch. 3 Output